REAL TIME DISCRETE FOURIER TRANSFORMS USING A PROGRAMMABLE DIODE-CONVOLVER MODULE*

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Abstract

A new surface acoustic wave delay line module is described which provides, for the first time, the ability to compute the real time Discrete Fourier Transform (DFT) with electronically variable bandwidth. Initial experiments with 12 and 32 tap PDC modules are described which demonstrated a 40 dB tap dynamic range and Fourier bandwidth variable from zero to beyond 10 MHz.

In microwave communications equipment, it is often important to be able to pass the incoming signal through a transform signal processor in order to put the signal into a form useful for information reception. Examples are radar pulse compression receivers, signal spectrum analysis, and multi-channel communication link decoding. For signals with bandwidth below 1 MHz digital computer processors utilizing the Discrete Fourier Transform (DFT) have found many applications since the introduction of efficient computation algorithms like the Fast Fourier Transform (Ref. 1). However, for signals with bandwidth much larger than 1 MHz, the cost, complexity, and size of digital computer processors rapidly becomes prohibitive.

In several recent papers (Refs. 2-4), it has been shown that Surface Acoustic Wave (SAW) delay line devices have the capability to efficiently perform DFT operations in a configuration that is relatively simple, small in size and weight, and should be inexpensive to mass produce. The use of SAW devices in DFT processors comes from the observation (Ref. 2) that a tapped delay line transversal filter is ideally suited to a DFT unit which uses the chirp-z algorithm (Ref. 5). To carry out this algorithm, the input signal is: 1) multiplied by a chirp signal, 2) convolved with a chirp, and 3) post multipled by a chirp. The processor simplification comes from the use of a SAW device in the convolution step; SAW transversal filter devices can be designed to process signals ranging from a few MHz to, perhaps, 100 MHz in a single delay line.

In the present paper, we describe a new type of SAW device DFT module, one which employs a parallel input-serial output configuration and which is capable of DFT operations with bandwidth electronically variable from zero to some tens of MHz. The latter feature is new and gives increased flexibility for processor applications.

The new DFT module is based on the use of a programmable version of the earlier reported Diode Correlator signal processing devices (Ref. 6-9). The Diode-Correlator performs the convolution of two input signals by use of nonlinear interaction in a diode-coupled, SAW tapped delay line. In the programmable Diode-Convolved (PDC), the convolution operation is electronically weighted by adjusting or programming the currents applied to individual diode-taps. Figure 1 shows a schematic view of the PDC device.

In operation as a DFT processor, the PDC performs the three operations of the chirp-z transform in a single nonlinear delay line interaction region of time length T. Chirp signals with bandwidth $B = \mu T/\pi$ and form $\exp(j\omega_i t \pm j\mu t^2)$ are applied to delay line Ports 1 and 2. The complex envelop emerging at Port 3 with carrier frequency $\omega_3 = \omega_2 - \omega_1$ has the serial product convolution form (Ref. 6,7).

$$V_3(t) = A \sum_{p=1}^{P} g_p V_1(t - p\Delta T) V_2^*(t + p\Delta T) \qquad (1)$$

where P is the number of delay line taps, $\Delta T = T/P$ is the transit time between taps, and g_p is the electronically programmed tap weight. We have used the phase synchronism condition, $\omega_1 + \omega_2 = 2\pi n/\Delta T$, in deriving the simple form of Eq. (1). The Port 3 voltage with chirp signal inputs is found from Eq. 1 to be

$$V_3(t) = A \sum_{p=1}^{P} g_p e^{-j4\mu p\Delta T t} \qquad (2)$$

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and at $t = m/2B = m\pi/2\mu\Delta TP$ this becomes

$$V_3(t) = A\sum_{p=1}^{P} g_p e^{-j2\pi mp/P} \qquad (3)$$

which, within a constant, is equal to the usual definition of the DFT.

A key factor in the usefulness of a DFT module is the dynamic range over which signals can be processed. The theory of Diode-Correlator devices (Refs. 7-9) shows that the tap weighting coefficients should vary as $1/I_{bp}^2$ where I_{bp} is the dc bias current at the p^{th} tap. Experiments were performed with a 12 tap PDC module to confirm this tap weight variation. The experimental device used a lithium niobate delay line and with 370 ns tap spacing. The diodes were discrete IN914 devices. The input chirp signals were applied at approximately 140 and 200 MHz; the DFT output at Port 3 was received at the difference frequency, 60 MHz. Figure 2 shows the variation in Port 3 power output as a function of the total diode bias when only 10 taps were used and all taps were biased equally. Note, that the power output follows the expected $1/I_b^4$ law accurately for P_3 ranging from -90 to -45 dBm. Thus, a tap dynamic range exceeding 40 dB is demonstrated.

Experiments to investigate the use of PDC modules with bandwidths up to and exceeding 10 MHz have recently been initiated using a 32 tap device with 37 ns tap spacing. This device also uses a lithium niobate delay line, but the diodes and tap bias resistors are fabricated in silicon-on-sapphire on 0.005 inch centers. In spite of some experimental flaws, the initial results with this wide bandwidth DFT module were quite encouraging. Figure 3 shows the Port 3 transform output when the Fourier bandwidth was 5 MHz and the tap weights were programmed to be equal. The output in this case is expected from Eq. 1 to have the sin x/x form with first nulls at ± 100 ns. This response is accurately reproduced in Fig. 3. The device functions smoothly for Fourier bandwidths ranging from zero to 10 MHz; however, significant transform distortion is seen for bandwidths above 5 MHz due to the malfunction of six taps in the present unit. With all taps working perfectly, the present device should be useful for bandwidths up to $B = 1/\Delta T = 27$ MHz.

In conclusion, we have demonstrated the operation of a new type of SAW device DFT module which performs DFT operations with electronically variable bandwidth. The parallel-input, serial output configuration is especially well suited for use in two dimensional DFT processors where P identical input DFT devices of length N would be used to drive the P taps of the PDC (Ref. 10). A DFT of length NP is thus formed with configuration of great flexibility and with only moderate signal processing complexity. Such DFT processors would be very attractive for wide bandwidth transforms of length greater than 1024.

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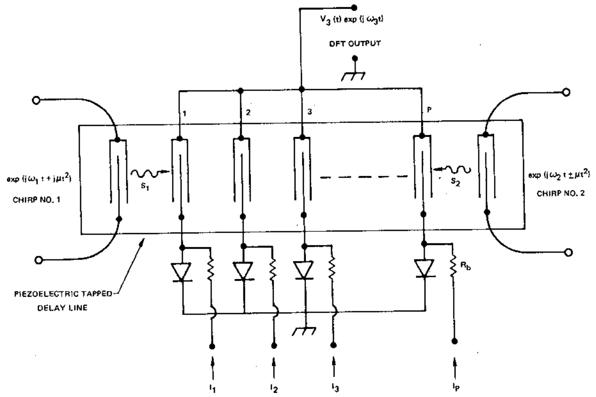

Fig. 1 - Schematic view of the Programmable Diode-Convolver DFT module

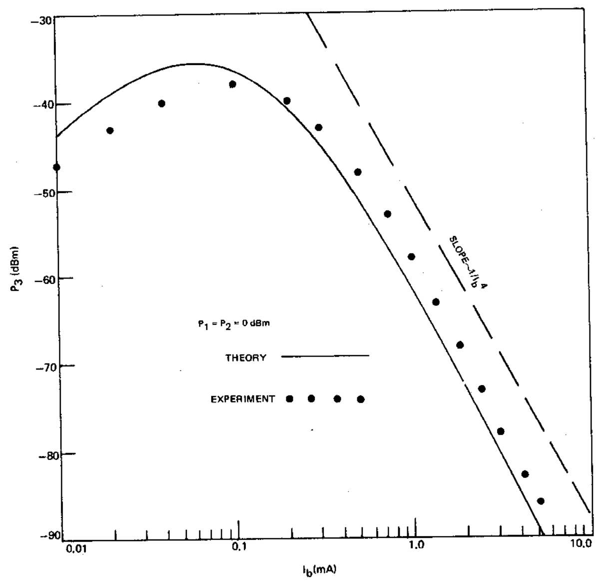

Fig. 2 - Variation in Port 3 output power versus diode bias current for a discrete diode PDC module

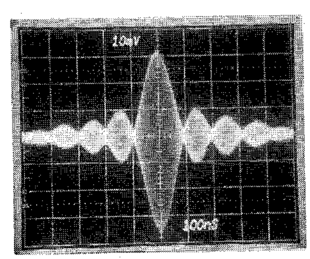

Fig. 3 - DFT output from a 32 tap PDC module using an SOS diode array (B = 5 MHz)